

BIPOLAR DIGITAL INTEGRATED CIRCUIT

μ PB1505GR

3.0 GHz PRESCALER DIVIDED BY 256, 128, 64 FOR BS/CS TUNER

DESCRIPTION

μ PB1505GR is a silicon prescaler IC operating up to 3.0 GHz and divided by 256, 128, 64. Due to 3.0 GHz operation and high division, this IC can contribute to produce BS/CS tuners with kit-use of 17K series DTS controller or standard CMOS PLL IC. The package is 8 pin plastic SOP suitable for surface mounting.

This IC is manufactured using NEC's 20 GHz fr NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect the chips from external pollution and prevent corrosion/migration. Thus, this IC has with excellent performance, uniformity and reliability.

FEATURES

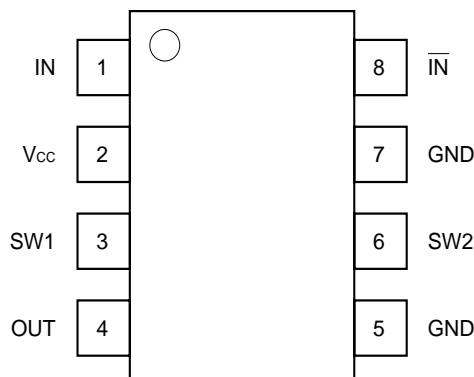
- High toggle-frequency : 0.5 GHz to 3.0 GHz
- Low power-consumption : 14 mA TYP. at 5 V
- High divide-ratio : $\div 256$, $\div 128$, $\div 64$
- High input-sensitivity : -14 to $+10$ dBm @ 1.0 GHz to 2.7 GHz
- Wide output-swing : 1.6 V_{p-p} (C_L = 8 pF load)

ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μ PB1505GR-E1	8 pin plastic SOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 k/reel Pin 1 is in tape pull-out direction.

Remarks To order evaluation samples, please contact your local NEC sales office. (Order number : μ PB1505GR)

PIN ASSIGNMENT (Top View)



Caution electro-static sensitive devices

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

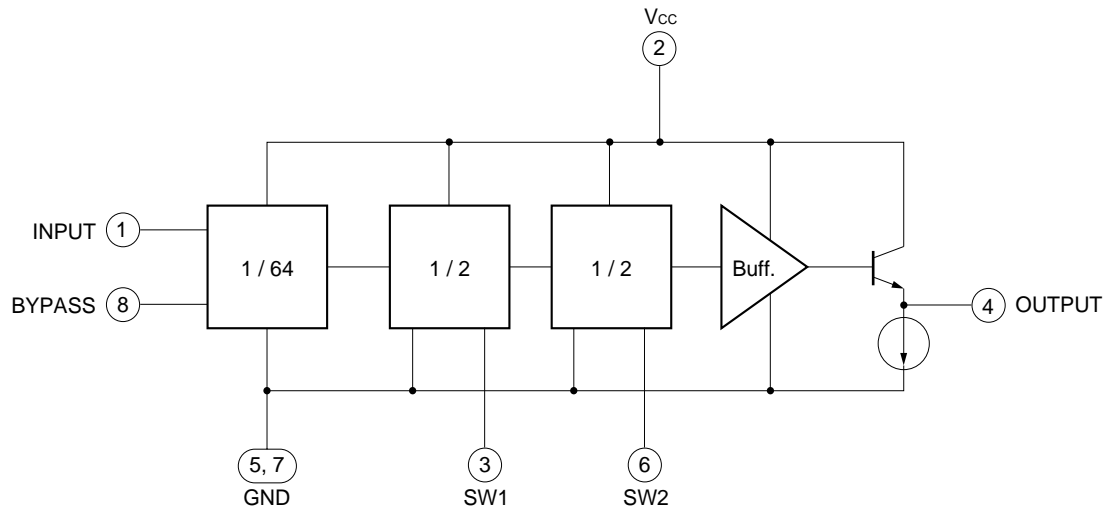
SELECTOR GUIDE

FEATURES	PRODUCT NUMBER	I _{cc} (mA)	f _{in} (GHz)	V _{cc} (V)	PACKAGE	PIN ASSIGNMENT
2.5 GHz / ± 512 , ± 256	μ PB586G	28	0.5 to 2.5	5	8 pin SOP	NEC original
2.5 GHz / ± 128 , ± 64	μ PB588G	26	0.5 to 2.5	5	8 pin SOP	
3.0 GHz / ± 256 , ± 128 , ± 64	μ PB1505GR	14	0.5 to 3.0	5	8 pin SOP	Typical of prescaler

Notice Typical performance. Please refer to Electrical Characteristics in detail.

To know the associated products, please refer to their latest data sheets.

INTERNAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	SYMBOL	ASSIGNMENT	FUNCTIONS AND EXPLANATION													
1	IN	Frequency input pin	Input frequency from an external VCO output. Must be coupled with capacitor (e.g. 1 000 pF) for DC cut.													
2	V _{cc}	Power supply pin	Supply voltage 5.0±0.5 V for operation. Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.													
3	SW1	Divided ratio control input pin 1	Divided ratio control can be governed by following input data to these pins. <table border="1"><tr><td colspan="2" rowspan="2"></td><td colspan="2">SW2</td></tr><tr><td>H</td><td>L</td></tr><tr><td rowspan="2">SW1</td><td>H</td><td>1/64</td><td>1/128</td></tr><tr><td>L</td><td>1/128</td><td>1/256</td></tr></table>			SW2		H	L	SW1	H	1/64	1/128	L	1/128	1/256
		SW2														
		H	L													
SW1	H	1/64	1/128													
	L	1/128	1/256													
6	SW2	Divided ratio control input pin 2														
4	OUT	Divided frequency output pin	This frequency output can be interfaced to CMOS PLL. Must be coupled with capacitor (e.g. 1 000 pF) for DC cut.													
5 7	GND	Ground pin	This pin must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible.)													
8	$\overline{\text{IN}}$	Frequency-input bypass pin	This pin must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.													

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	CONDITIONS
Supply voltage	V_{CC}	−0.5 to +6	V	$T_A = +25\text{ }^{\circ}\text{C}$
Input voltage	V_{IN}	−0.5 to $V_{CC} + 0.5$	V	$T_A = +25\text{ }^{\circ}\text{C}$
Power dissipation	P_D	250	mW	Mounted on $50 \times 50 \times 1.6$ mm double copper clad epoxy glass PWB ($T_A = +85\text{ }^{\circ}\text{C}$)
Operating temperature	T_{opt}	−40 to +85	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	−55 to +150	$^{\circ}\text{C}$	

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature	T_{opt}	−40	+25	+85	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = -40$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 4.5$ to 5.5 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Circuit current	I_{CC}	9.0	14.0	19.5	mA	No input signal
Upper response frequency 1	$f_{in(U)1}$	3.0			GHz	$P_{in} = -10$ to $+10$ dBm
Upper response frequency 2	$f_{in(U)2}$	2.7			GHz	$P_{in} = -14$ to -10 dBm
Lower response frequency 1	$f_{in(L)1}$			0.5	GHz	$P_{in} = -10$ to $+8$ dBm
Lower response frequency 2	$f_{in(L)2}$			1.0	GHz	$P_{in} = -14$ to -10 dBm, $+8$ to $+10$ dBm
Input sensitivity 1	P_{in1}	−10		+8	dBm	$f_{in} = 0.5$ to 1.0 GHz
Input sensitivity 2	P_{in2}	−14		+10	dBm	$f_{in} = 1.0$ to 2.7 GHz
Input sensitivity 3	P_{in3}	−10		+10	dBm	$f_{in} = 2.7$ to 3.0 GHz
Output Swing	V_{OUT}	1.3	1.6		V_{P-P}	$C_L = 8$ pF
SW1 input voltage (H)	V_{IH1}	V_{CC}	V_{CC}	V_{CC}	V	
SW1 input voltage (L)	V_{IL1}	OPEN	OPEN	OPEN	V	
SW2 input voltage (H)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	V	
SW2 input voltage (L)	V_{IL2}	OPEN	OPEN	OPEN	V	

TEST CIRCUIT

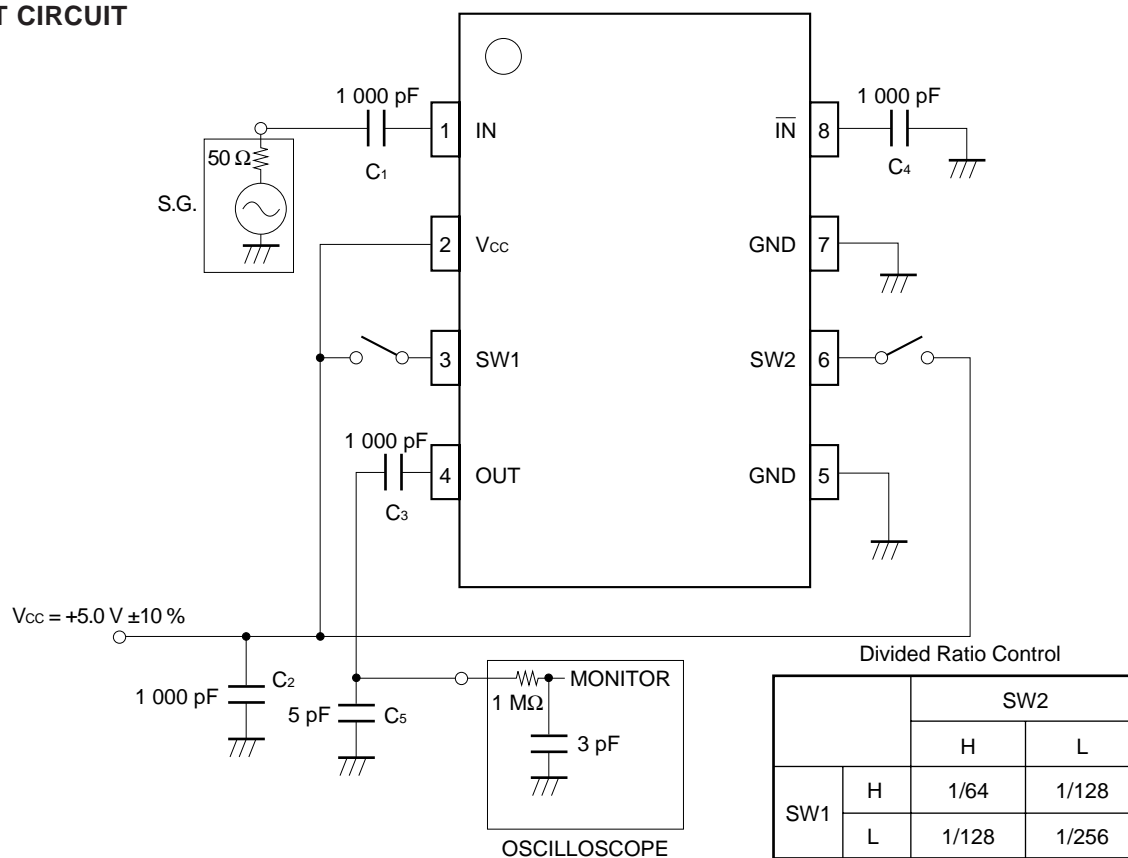
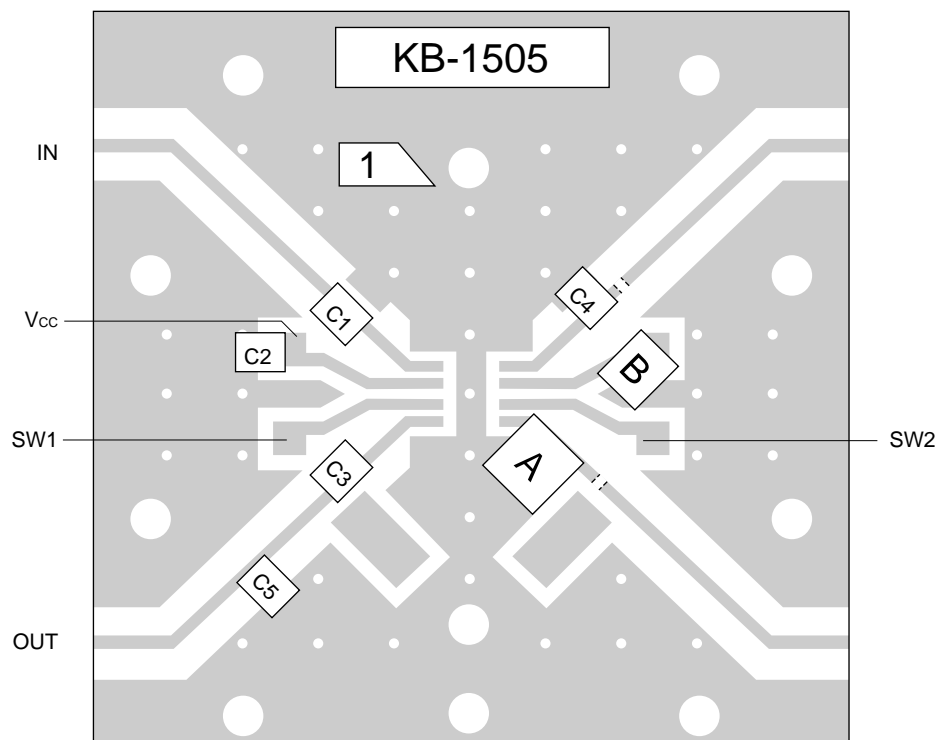


ILLUSTRATION OF TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD

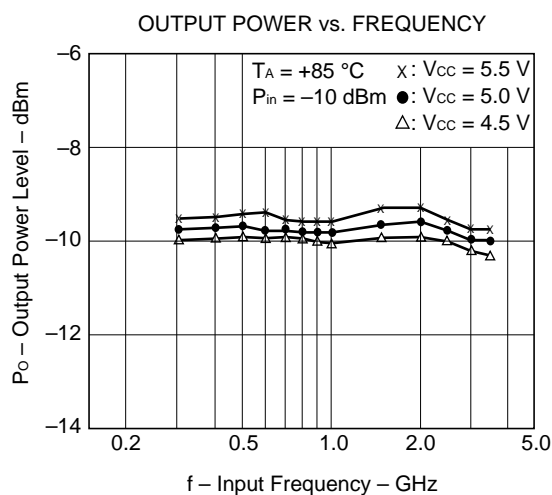
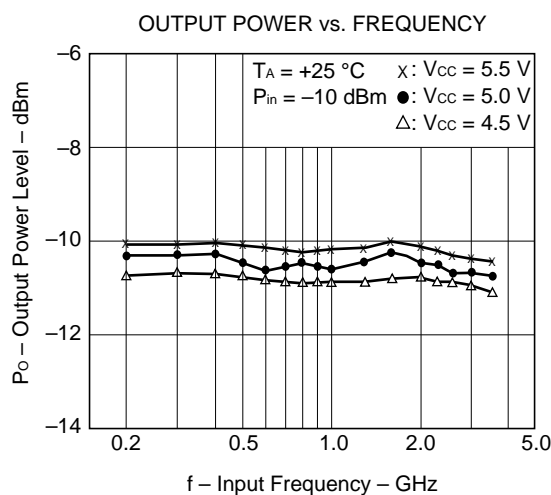
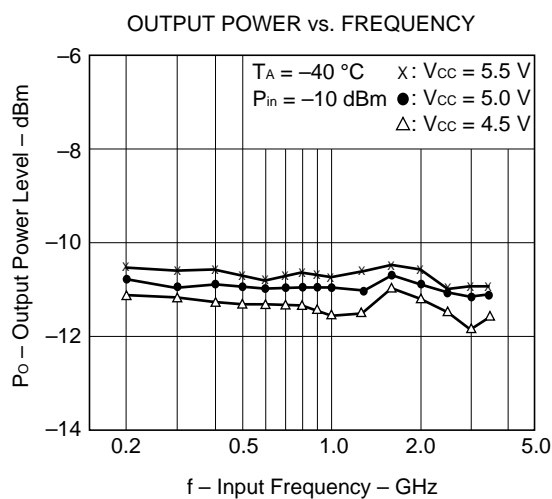
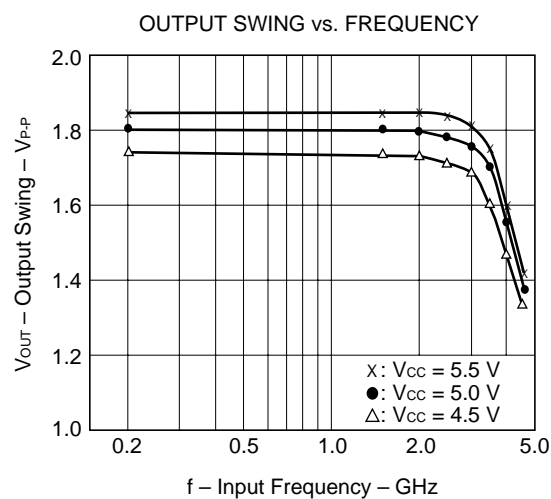
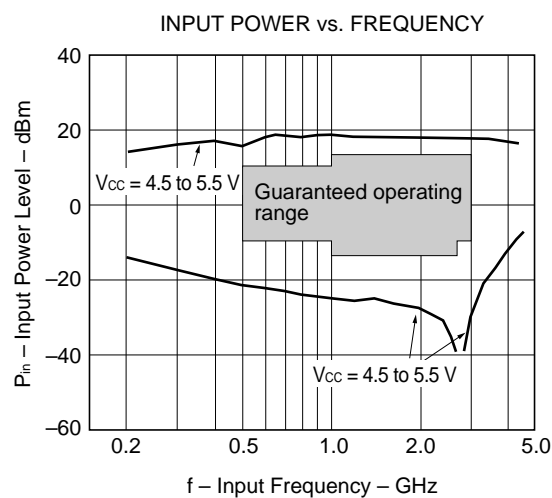
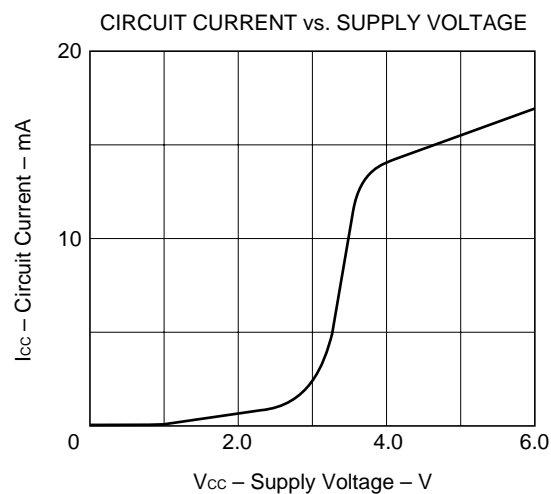


COMPONENT LIST

No.	Value
C1 to C4	1 000 pF
C5	5 pF
A, B	shorting chip

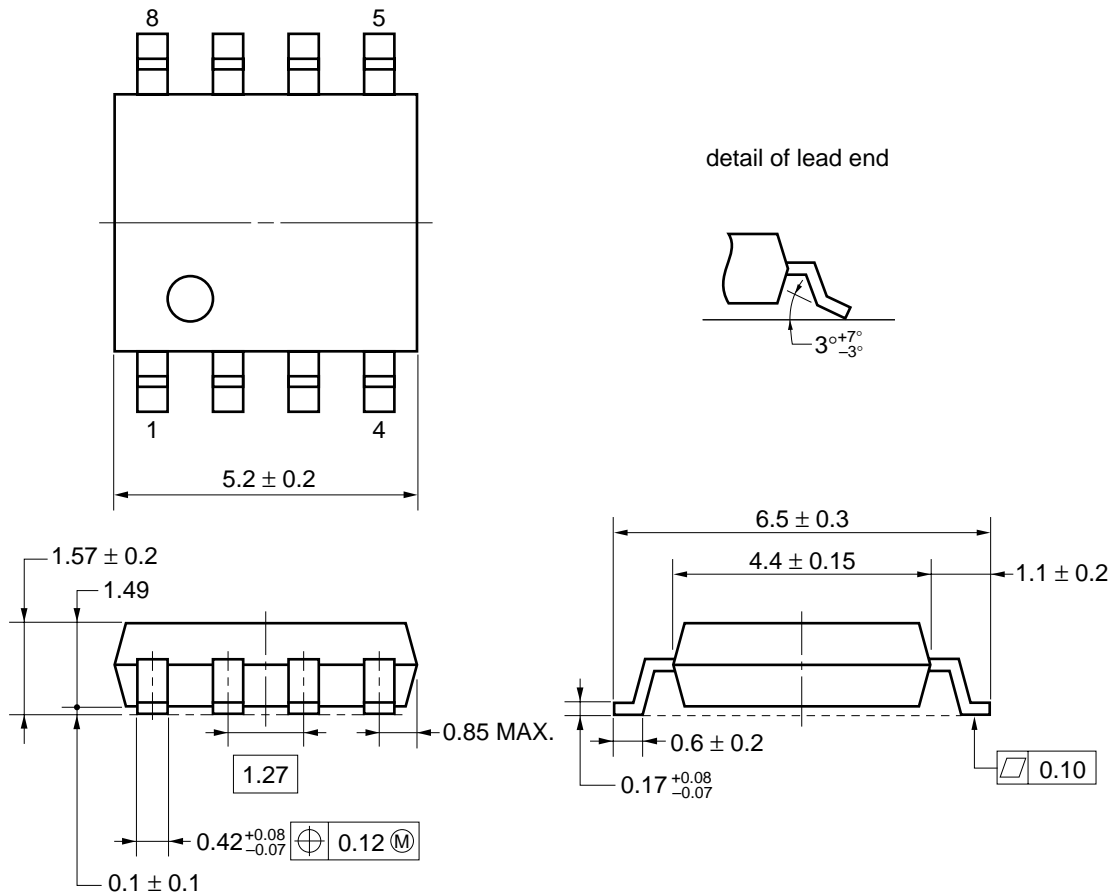
Note :

- (*1) 50 × 50 × 0.4 mm double copper clad polyimide board
- (*2) Back side : GND pattern
- (*3) Solder plated on pattern
- (*4) ○ : Through holes
- (*5) ; ; pattern should be removed on this testing.

TYPICAL CHARACTERISTICS (Unless otherwise specified $T_A = +25\text{ }^{\circ}\text{C}$)

PACKAGE DIMENSIONS

★ 8 PIN PLASTIC SOP (225 mil) (UNIT: mm)



NOTE Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

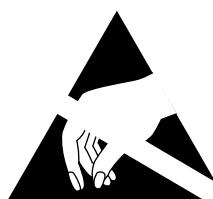
μ PB1505GR

Soldering method	Soldering conditions	Recommended conditoin symbol
Infrared ray reflow	Package peak temperature : 235 °C, Hour : within 30 s. (more than 210 °C), Time : 3 time, Limited days : no. *	IR35-00-3
VPS	Package peak temperature : 215 °C, Hour : within 40 s. (more than 200 °C), Time : 3 time, Limited days : no. *	VP-15-00-3
Wave soldering	Soldering tub temperature : less than 260 °C, Hour : within 10 s. Time : 1 time, Limited days : no. *	WS60-00-1
Pin part heating	Pin area temperature : less than 300 °C, Hour : within 3 s./pin Limited days : no. *	

* : It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Note 1. The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).



ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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