



National Semiconductor

July 1989

DM54LS469/DM74LS469 8-Bit Up/Down Counter

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General Description

The 'LS469 is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs (\overline{LD} , \overline{UD} , \overline{CBI}) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

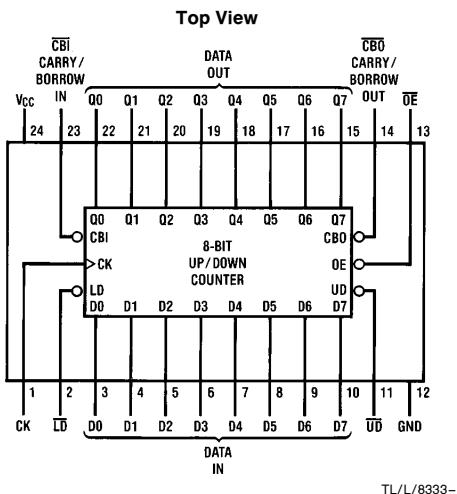
The LOAD operation loads the inputs (D_7 - D_0) into the output register (Q_7 - Q_0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE (\overline{CBI} =LOW), otherwise the operation is a HOLD. The carry-out (CBO) is TRUE (CBO =LOW) when the output register (Q_7 - Q_0) is all HIGHs, otherwise FALSE (CBO =HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE (CBI =LOW), otherwise the operation is a HOLD. The borrow-out (CBO) is TRUE (CBO =LOW) when the output register (Q_7 - Q_0) is all LOWs, otherwise FALSE (CBO =HIGH).

The output register (Q_7 - Q_0) is enabled when \overline{OE} is LOW, and disabled (HI-Z) when \overline{OE} is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469 octal up/down counters may be cascaded to provide larger counters.

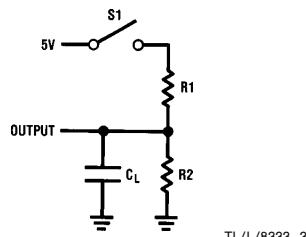
Features/Benefits

- 8-bit up/down counter for microprogram-counter, DMA controller and general-purpose counting applications
- 8 bits matches byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Connection Diagram



Standard Test Load



TL/L/8333-3

Order Number DM54LS469J,
DM74LS469J or DM74LS469N
See NS Package Number J24F or N24C

Function Table

\overline{OE}	CK	\overline{LD}	\overline{UD}	\overline{CBI}	D_7 - D_0	Q_7 - Q_0	Operation
H	X	X	X	X	X	Z	HI-Z
L	\uparrow	L	X	X	D	D	LOAD
L	\uparrow	H	L	H	X	Q	HOLD
L	\uparrow	H	L	L	X	Q plus 1	INCREMENT
L	\uparrow	H	H	H	X	Q	HOLD
L	\uparrow	H	H	L	X	Q minus 1	DECREMENT

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Off-State Output Voltage 5.5V
Storage Temperature -65°C to +150°C

Supply Voltage V_{CC} 7V
Input Voltage 5.5V

Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T _A	Operating Free-Air Temperature	-55		125*	0		75	°C
t _w	Width of Clock	Low	40		35	10		ns
		High	30		25			
t _{su}	Set Up Time	60			50			ns
t _h	Hold Time	0	-15		0	-15		

*Case Temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V _{IL}	Low-Level Input Voltage						0.8	V
V _{IH}	High-Level Input Voltage				2			V
V _{IC}	Input Clamp Voltage	V _{CC} =MIN	I _I = -18 mA				-1.5	V
I _{IL}	Low-Level Input Current	V _{CC} =MAX	V _I =0.4V				-0.25	mA
I _{IH}	High-Level Input Current	V _{CC} =MAX	V _I =2.4V				25	μA
I _I	Maximum Input Current	V _{CC} =MAX	V _I =5.5V				1	mA
V _{OL}	Low-Level Output Voltage	V _{CC} =MIN	MIL	I _{OL} =12 mA			0.5	V
		V _{IL} =0.8V	COM	I _{OL} =24 mA				
V _{OH}	High-Level Output Voltage	V _{CC} =MIN	MIL	I _{OH} = -2 mA	2.4			V
		V _{IL} =0.8V	COM	I _{OH} = -3.2 mA				
I _{OZL}	Off-State Output Current	V _{CC} =MAX		V _O =0.4V			-100	μA
		V _{IL} =0.8V		V _O =2.4V			100	μA
I _{OS}	Output Short-Circuit Current*	V _{CC} =5.0V		V _O =0V	-30		-130	mA
I _{CC}	Supply Current	V _{CC} =MAX				120	180	mA

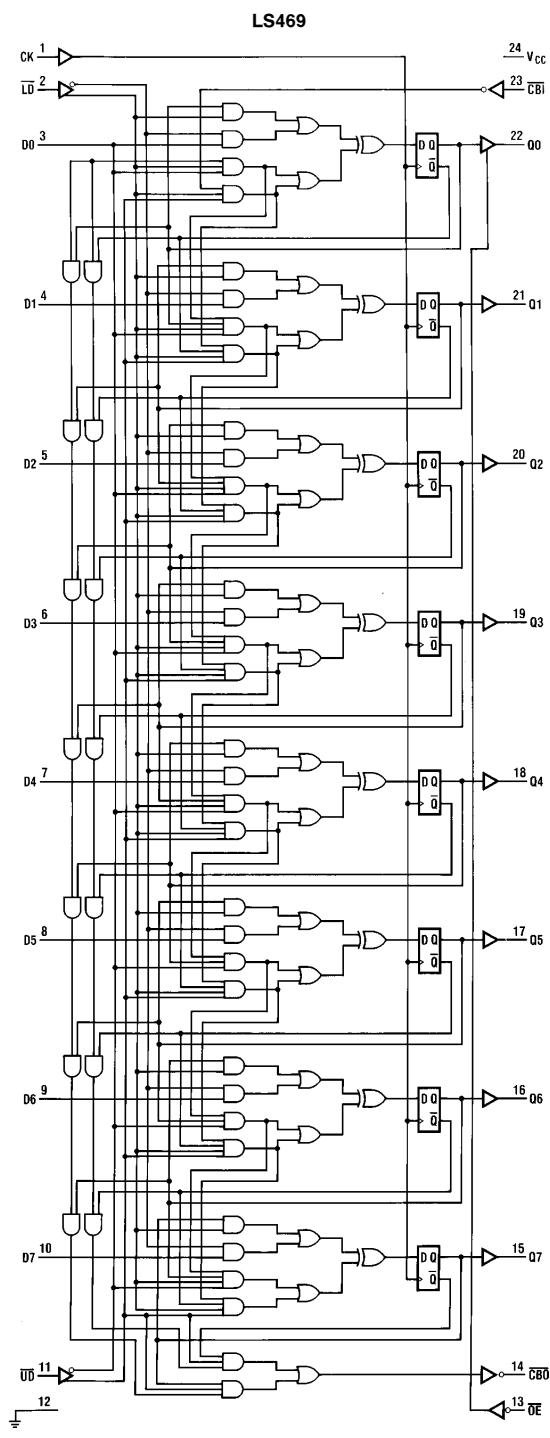
*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

† All typical values are V_{CC}=5V, T_A=25°C.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load/Waveforms)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f _{MAX}	Maximum Clock Frequency	C _L =50 pF R ₁ =200Ω R ₂ =390Ω	10.5			12.5			MHz
	CBI to CBO Delay			35	60		35	50	ns
	Clock to Q			20	35		20	30	ns
	Clock to CBO			55	95		55	80	ns
	t _{PZX} Output Enable Delay			20	45		20	35	ns
	t _{pxz} Output Disable Delay			20	45		20	35	ns

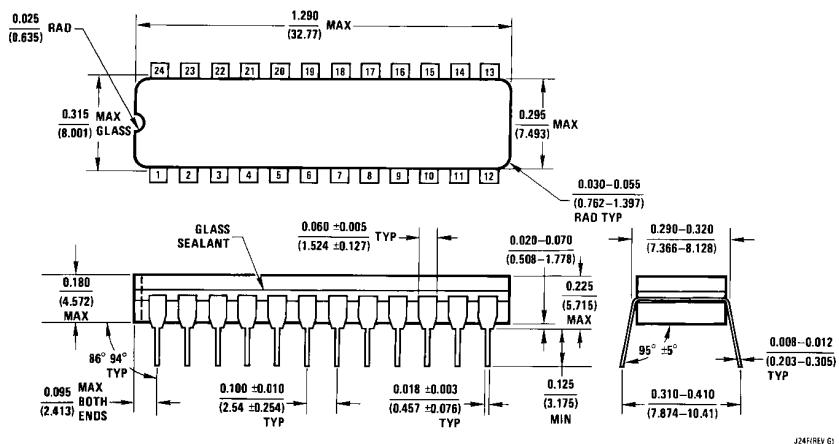
Logic Diagram



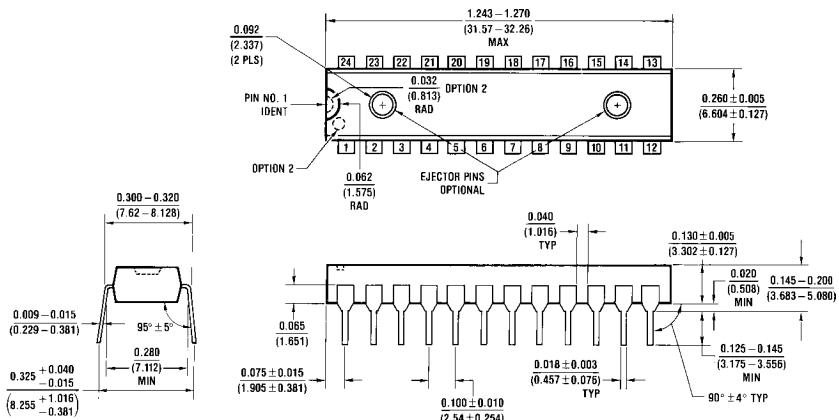
TL/L/8333-2

DM54LS469/DM74LS469 8-Bit Up/Down Counter

Physical Dimensions inches (millimeters)



**24-Pin Narrow Ceramic Dual-In-Line Package (J)
Order Number DM54LS469J or DM74LS469J
NS Package Number J24F**



**24-Pin Narrow Plastic Dual-In-Line Package (N)
Order Number DM74LS469N
NS Package Number N24C**

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 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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